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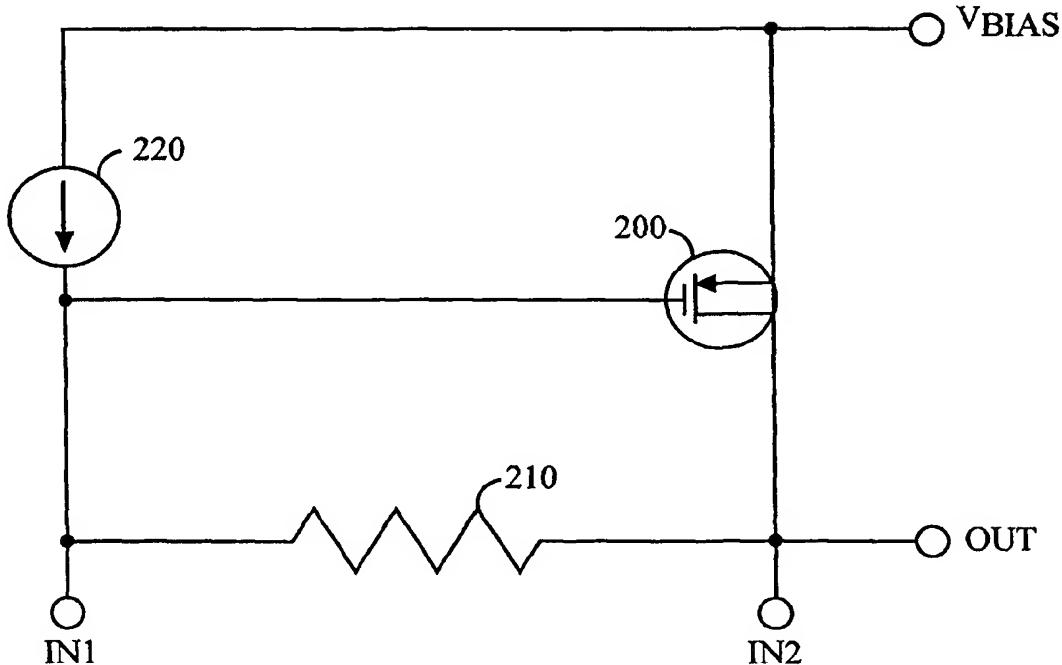
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(54) Title: ACTIVE DIFFERENTIAL TO SINGLE-ENDED CONVERTER



(57) Abstract

Many applications require the conversion of a differential current signal into a single-ended signal. The shortcomings encountered with existing approaches include poor conversion efficiency, limited bandwidth, and large size. The converter disclosed uses active devices to obtain a unit of small size and high efficiency having a wide bandwidth of operation.

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ACTIVE DIFFERENTIAL TO SINGLE-ENDED CONVERTER

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BACKGROUND OF THE INVENTION

This invention relates to circuits for converting or combining signals, and specifically to circuits for converting differential signals into single-ended signals. More specifically, this invention relates to the conversion of a differential alternating current signal into a single-ended signal.

I. Field of the Invention

II. Description of Related Art and General Background

Conversion of a differential signal to a single-ended signal is used in many different circuit applications. Due to their immunity to common-mode interferences, differential signals are often used to interconnect electronic devices. The differential signals are then converted to single-ended signals for transmission by wire or wireless means. Differential signals are also often used in frequency conversion devices to reject local oscillator leakage and other spurious responses.

A simple converter which uses an inductive transformer is illustrated in FIG. 1. With the inductors coupled as indicated, changes in the currents flowing through the primary coils 10 and 20 induce voltages across the secondary coils 30 and 40, respectively, according to the well-known relation

25

$$v = M \times di/dt \quad (1)$$

where M is a constant factor defining the degree of coupling between the primary and secondary coils. As a consequence of relation (1), the circuit of FIG. 1 operates by converting a time-varying difference between input currents IN_1 and IN_2 into an output voltage OUT . For most applications, coils 10 and 20 will be identical to each other, and coils 30 and 40 will also be identical to each other, so that each input signal will encounter the same impedance and will undergo conversion by the same factor M .

FIG. 2 shows a representative use for such a converter. A differential voltage signal Δ , having a (possibly zero) DC offset component Δ_{dc} and a small-signal AC component Δ_{ac} , is inputted to the base terminals of a

differential pair of active devices **50** and **60**. The emitters of active devices **50** and **60** are connected together and biased by direct current source **70**. The collectors of active devices **50** and **60** are biased through their connections to the terminals of the primary coils **10** and **20**, between which coils is applied a
5 DC bias voltage V_{bias} .

Because source **70** is assumed ideal, all AC current flow is confined to the loop formed by active devices **50** and **60** and the primary coils **10** and **20**. As the amplitude of signal Δ_{ac} fluctuates between positive and negative, the bias current flows through the loop first in one direction and then in the other,
10 inducing a corresponding AC voltage in the secondary windings according to relation (1) above.

The size of an inductive transformer is inversely proportional to the frequency of operation. This factor makes such transformers unsuitable for many low-frequency applications, including those in the VHF-UHF frequency
15 range. For example, a discrete inductive transformer for operation at these frequencies may be as large as 3.8 mm × 3.8 mm × 3.8 mm.

When one attempts to integrate such devices onto the circuit chip instead, a different set of problems arises. One such problem is poor coupling between the primary and secondary coils (i.e. a low value of M), which results
20 in low conversion efficiency. Other problems include dissipative loss in metal conductors; losses due to low substrate resistance, including those caused by capacitative and magnetic coupling of the inductor to the substrate; and a large occupied chip area thereby increasing the cost of the entire integrated circuit.

25 At RF frequencies, the differential to single-ended conversion may also be performed by using a half-wavelength transmission line. In the VHF and UHF ranges, however, this approach is not feasible for many applications because of the physical length of the line required (even at $f = 1$ GHz, for example, $\lambda/2 = 15$ cm). In such cases, a lumped equivalent circuit such as the
30 LCL pi network shown in FIG. 3 may be used to create the same effect. Note that while a LCL version is shown here, a CLC version may also be used to obtain the same result.

In contrast to the inductive transformer described above, which converts input currents to an output voltage, the half-wavelength
35 transmission line and the equivalent pi circuit of FIG. 3 work by inverting the phase of one of the input currents. As described in the technical article "Current combiner enhances active mixer performance" by Alvin K. Wong, Sheng H. Lee, and Michael G. Wong, *Microwaves & RF*, March 1994, pp. 156-

165, which article is hereby incorporated by reference, this operation may be verified through the following decomposition of FIG. 3:

- 5 • obtain the equivalent circuit in FIG. 4A by applying two AC current sources having the same magnitude i but 180 degrees out of phase at nodes IN1 and IN2, replacing capacitor 130 (of value C) with its equivalent of two capacitors 131 and 132 (each of value 2C) connected in series, and noting that the inductors 110 and 120 are shunts to ground for AC signals;
- 10 • replace the parallel combination of the current source applied at node IN1 (of value i) and inductor 110 (of value L) with its Thévenin equivalent of a series combination of a voltage source of value $i \times j\omega L$ and an inductor of value L;
- 15 • note that at resonant frequency ω_0 , the series combination of an inductor of value L and capacitor 131 (of value 2C) appears to be a short circuit, and perform this substitution to obtain FIG. 4B;
- 20 • replace the series combination of the voltage source of value $i \times j\omega L$ and capacitor 132 (of value 2C) with its Norton equivalent of a parallel combination of a current source of value $-i\omega^2 L 2C$ and a capacitor of value 2C;
- 25 • note that at resonant frequency ω_0 , the parallel combination of inductor 120 (of value L) and a capacitor of value 2C appears to be an open circuit, and perform this substitution to obtain FIG. 4C;
- note that at resonant frequency ω_0 , the expression $-i\omega^2 L 2C$ reduces to $-i$, and substitute $-i$ for the value of the current source obtained in the previous step. By changing $-i$ to i in order to reverse the direction of the current flow arrow for this source, we see that the two sources in FIG. 4C are identical and that their currents add in sum at output node OUT.

30 In this way the circuit changes the phase of the current applied to IN1 to match that of the current applied at IN2 and thus combines the two currents.

As a representative use for such a converter, FIG. 5 shows a downconverter mixer which converts an input RF signal to a intermediate frequency (IF). A local oscillator (not shown) produces a differential voltage signal of frequency f_{LO} defined as the voltage between V_{LO+} and V_{LO-} . This voltage signal is converted into an alternating bias current by differential pair 50 and 60. Input RF signal m is applied to the base of current source 80, causing the bias current of the active devices 50 and 60 to vary with the

amplitude of m as well as with the amplitude of the differential signal. In this case, f_{LO} is chosen so that $f_{LO} > f_m$. The output signal at node OUT thus contains a component at frequency ($f_{LO} + f_m$), which is removed by lowpass filtering (not shown), and another component at the intermediate frequency 5 ($f_{LO} - f_m$) which is modulated in substantially the same fashion as input signal m .

Although a discrete implementation of this lumped equivalent circuit is much smaller than an inductive transformer or a half-wavelength transmission line for the same frequency, it would still be relatively large for 10 use in the VHF-UHF range because of the inductors. Such use of off-chip components would also cause additional fabrication and assembly costs.

This circuit would not be suitable for integration either, although in this case no inductive coupling is needed. Inductors fabricated on IC chips suffer from a poor 'quality factor' (or 'Q factor'), calculated as the ratio of 15 reactance to resistance and defined as the ratio of the energy stored by the circuit per cycle of the resonant frequency to the power dissipated by the circuit [i.e., $(\omega \times E_{st})/P_{diss}$]. In order to compensate for this shortcoming, wide inductor traces must be used to reduce resistive loss. An increase in trace width, however, results in a squared increase in chip area consumed. 20 Moreover, in order to avoid crosstalk, other signal traces cannot be placed over this area and must be routed around it instead, causing additional problems in circuit layout and space utilization efficiency.

A chip-level inductor having an increased area encounters other problems as well. The silicon substrate is conductive, so AC current flow in 25 the coil generates eddy currents in the substrate. The resulting dissipative losses increase with the area covered by the coil. Therefore, on-chip fabrication of inductors requires a tradeoff between several detrimental effects, and the end result is that high-Q components cannot be obtained.

Because of the factors described above, the practical upper limit for 30 inductors on silicon chips is approximately 15 to 20 nH. For applications in the VHF range, however, inductances of hundreds of nanohenrys are required. For example, to achieve the differential-to-single-ended conversion at 70 MHz using the circuit in FIG. 3, with capacitor 130 having a value of 130 pF, the value of each inductor 110 and 120 should be 258.5 nH. Therefore, 35 monolithic implementation of this converter for use in RF applications at such frequencies is not feasible.

In addition to these implementational barriers, problems also arise regarding the performance of this converter circuit. For example, the loading

of the inputs is not symmetrical, as the input at node IN1 sees a larger impedance than the input at node IN2. This effect causes a circuit imbalance, reducing the common-mode rejection by the circuit and making it prone to common-mode interferences or noise. In mixers, this imbalance would also
5 affect such important characteristics as rejection of the local oscillator leakage and other spurious responses. Also, the 180-degree phase shift of the current at node IN1 is strictly valid only at ω_0 , so the conversion occurs only in a very narrow frequency range determined by the loaded Q factor of the LC resonators. Moreover, additional passive components are required to match
10 the output impedance to the load impedance.

SUMMARY OF THE INVENTION

A converter after the present invention contains no inductors and can
15 readily be implemented in any IC fabrication process. Because the input impedances are equal, the inputs are symmetrically loaded and a balanced operation is maintained. High output efficiency is realized by matching the output impedance to the load impedance without requiring additional components. The circuit's operating bandwidth is also much wider than for
20 the purely reactive converters described above. The conversion gain can easily be increased without disrupting the output-to-load impedance match, so long as the signal frequency is within the operating bandwidth, simply by changing the value of a circuit resistance.

25 BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a first example of a converter in the related art.
FIG. 2 is a representative application for the converter of FIG. 1.
FIG. 3 is a second example of a converter in the related art.
30 FIG. 4A is a small-signal equivalent of the circuit in FIG. 3.
FIG. 4B is an equivalent of the circuit in FIG. 3.
FIG. 4C is another equivalent of the circuit in FIG. 3.
FIG. 5 is a representative application for the converter of FIG. 3.
FIG. 6 is an illustration of a circuit after the first embodiment of the
35 invention.
FIG. 7 is a complementary version of the circuit in FIG. 6.
FIG. 8 is a small-signal equivalent of the circuit in FIG. 6.

FIG. 9 is an illustration of a circuit after the first embodiment of the invention in normal operation.

FIG. 10 is an illustration of a circuit after the second embodiment of the invention.

5 FIG. 11 is an illustration of a degenerated-emitter bipolar junction transistor.

DETAILED DESCRIPTION OF THE INVENTION

10 As shown in FIG. 6, the first embodiment of the invention comprises an active device 200 in a common-source configuration, with the gate and drain of active device 200 connected to the first and second signal inputs, respectively. The drain of active device 200 is also connected to the single-ended signal output. A resistance 210 is added between the input nodes IN1 and IN2 to provide a closed-loop path for the input AC current, and a DC current source 220 supplies current from the node at potential V_{bias} to input node IN1. A complementary version of the first embodiment is shown in FIG. 7.

20 Operation of this circuit is different than that of either related art circuit discussed above. Specifically, it does not operate by the inductive conversion of current to voltage (as there are no inductors), or by inverting the phase of any current.

25 Consider the small-signal equivalent circuit as shown in FIG. 8. As source 320 is assumed ideal, no AC current flows through it. Also, DC bias node V_{bias} is effectively at AC ground potential. To determine the circuit's output impedance, we leave the inputs unconnected. Because no current flows through resistor 210, nodes IN1, IN2, and OUT and the gate and drain terminals of active device 200 are all at the same potential.

30 An AC voltage v_{test} applied at node OUT causes active device 200 to generate a current $g_m \times v_{test}$ ($= -g_m \times v_{gs}$) flowing through node OUT. Therefore, the impedance of the circuit is $1/g_m$, where g_m is the transconductance of the active device 200. By choosing g_m to be the reciprocal of the load impedance, we thus match the output and load impedances without adding any components that could affect the circuit's conversion efficiency.

35 In normal operation, nodes IN1 and IN2 are driven by a pair of AC current sources which have the same magnitude and are 180 degrees out-of-phase (active devices 50 and 60 in FIG. 2 are one example of such a pair).

Assume that current i_{IN1} flows out of node IN1, while current i_{IN2} flows into node IN2, as shown in FIG. 9. As the only available AC path for current i_{IN1} is through resistance 210, it follows that current i_{IN1} flows out of node IN2. Because $i_{IN1} = i_{IN2}$, we may assume that all of the AC input current flows 5 through resistance 210, and that none of it flows through the active device 200 or through the load.

Thus we can see that the current generated by the active device 200, $g_m \times v_{gs}$, flows only through the load, thereby creating a voltage $g_m \times v_{gs} \times R_L$ at node OUT, which is the same node as node IN2. Because we have chosen g_m 10 to be $1/R_L$, it follows that $v_{IN2} = v_{gs}$. Further, because $v_{gs} = -v_{IN1}$, we have $v_{IN2} = -v_{IN1}$. Now, as i_{IN1} and i_{IN2} are equal but antiparallel, we can obtain such equal but antiparallel input voltages only as a result of equal input impedances at nodes IN1 and IN2. In other words, $Z_{IN1} = Z_{IN2}$, and the circuit is balanced in normal operation.

15 The conversion gain of the circuit is the ratio of the voltage at node OUT to the input differential current signal. Because our input signal flows only through resistance 210, we can express it as the ratio of the voltage drop across resistance 210 to the value of resistance 210 (which we now designate as R). Knowing that the voltage at node OUT is v_{IN2} , we can therefore express 20 the conversion gain as $(v_{IN2} \times R) / (v_{IN2} - v_{IN1})$. As $v_{IN2} = -v_{IN1}$, we conclude that the conversion gain of the circuit is $R/2$.

At high frequencies, a complete analysis of the circuit's performance will take the capacitances of the active device into account. We therefore consider the effect of the most significant of these capacitances: the gate-source capacitance C_{gs} . We first determine ω_T , the frequency of unity current 25 gain for the active device, where $\omega_T = g_m / C_{gs}$. For PMOS and PNP devices, ω_T is typically in the range of 200-300 MHz, while for NMOS and NPN devices ω_T is typically 20-60 GHz.

We may now obtain the following modified expression for the 30 conversion gain of the circuit:

$$\frac{R}{2} \cdot \frac{1 + \frac{j\omega}{\omega_T}}{1 + \frac{j\omega}{2\omega_T} \left(1 + \frac{R}{R_L} \right)}.$$

We may also obtain the 3 dB bandwidth for the circuit as

$$\omega_{3dB} = \frac{\omega_T}{\sqrt{\frac{1}{4} \left(1 + \frac{R}{R_L} \right) - 2}}.$$

Given the typical values for ω_t noted above, we may easily see that by proper selection of R, we may obtain a very large value for ω_{3dB} , much larger than any such value that may be obtained with the circuit of FIG. 3.

5 Note that the DC current source 220 does not appear in the small-signal analysis, as it serves only to provide bias current to the source connected to node IN1. As such, it may comprise any circuit which passes DC but has a high impedance at the operating frequencies, such as a parallel LC resonator or a quarter-wavelength transmission line.

10 The novel circuit herein described may be used in conjunction with any circuit producing a differential current signal: for example, a differential gain stage or a balanced mixer. Likewise, the active device 200 is not limited to an insulated-gate FET or MOSFET as shown, but is equally suitable for use with any other device that may be configured as a voltage-dependent current source, such as a FET, a bipolar junction transistor (BJT), a heterojunction BJT 15 fabricated e.g. in GaAs or SiGe, a MESFET, a high-electron-mobility transistor (HEMT), or a degenerated transistor of any of these types. An example of a degenerated-emitter BJT suitable for use as active device 200 is illustrated in FIG. 11.

20 In some applications, the current supplied by active device 200 may be insufficient as a DC bias current for the device connected to node IN2. In such cases, the second embodiment of the invention may be used. In this embodiment, as illustrated in FIG. 10, a second DC current source 230 is used to supplement the DC current available at node IN2. As noted above with respect to the first DC current source, this second DC current source does not 25 appear in the small-signal analysis and may comprise any circuit which passes DC but has a high impedance at the operating frequencies.

30 The foregoing description of the preferred embodiments is provided to enable any person skilled in the art to make or use the present invention. Various modifications to these embodiments will be readily apparent to those skilled in the art, and the generic principles presented herein may likewise be applied to other embodiments without use of the inventive faculty. Thus, the present invention is not intended to be limited to the embodiments shown above but rather is to be accorded the widest scope consistent with the principles and novel features disclosed in any fashion herein.

35 **WHAT IS CLAIMED IS:**

CLAIMS

1. A circuit for converting a differential current signal to a single-ended signal, comprising:
2 an active device having a control terminal, a charge-producing terminal, and a charge-collecting terminal; and
4 a resistance having two terminals;
6 wherein a bias potential is applied at least indirectly to the charge-producing terminal of said active device; and
8 wherein one of the two terminals of said resistance is connected to the charge-collecting terminal of said active device, and the other of the two terminals of said resistance is connected to the control terminal of said active device; and
10 wherein the differential current signal is applied to the terminals of the resistance, and the single-ended signal is outputted at the charge-collecting terminal of said active device.

2. A circuit for converting a differential current signal to a single-ended signal according to claim 1, wherein said active device is a field-effect transistor.

3. A circuit for converting a differential current signal to a single-ended signal according to claim 1, wherein said active device is a bipolar junction transistor.

4. A circuit for converting a differential current signal to a single-ended signal according to claim 1, wherein said active device is selected from the group consisting of a metal-semiconductor field-effect transistor, a heterojunction bipolar junction transistor, and a high-electron-mobility transistor.

5. A circuit for converting a differential current signal to a single-ended signal according to claim 1, further comprising a direct current source having two terminals,

4 wherein the bias potential is applied to one of the two terminals of said direct current source, and the other of the two terminals of said direct current source is connected to the control terminal of said active device.

6. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said active device is a field-effect transistor.

7. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said active device is a bipolar junction transistor.

8. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said active device is selected from the group consisting of a metal-semiconductor field-effect transistor, a heterojunction bipolar junction transistor, and a high-electron-mobility transistor.

9. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said direct current source comprises a high-impedance circuit.

10. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said direct current source comprises a resonant circuit having an inductor and a capacitor connected in parallel to said inductor, wherein said resonant circuit has a high impedance.

11. A circuit for converting a differential current signal to a single-ended signal according to claim 5, wherein said direct current source comprises a quarter-wavelength transmission line.

12. A circuit for converting a differential current signal to a single-ended signal according to claim 1, further comprising a direct current source having two terminals,

4 wherein the bias potential is applied to one of the two terminals of said direct current source, and the other of the two terminals of said direct current source is connected to the charge-collecting terminal of said active device.

13. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said active device is a field-effect transistor.

14. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said active device is a bipolar junction transistor.

15. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said active device is selected from the group consisting of a metal-semiconductor field-effect transistor, a heterojunction bipolar junction transistor, and a high-electron-mobility transistor.

16. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said direct current source comprises a high-impedance circuit.

17. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said direct current source comprises a resonant circuit having an inductor and a capacitor connected in parallel to said inductor, wherein said resonant circuit has a high impedance.

18. A circuit for converting a differential current signal to a single-ended signal according to claim 12, wherein said direct current source comprises a quarter-wavelength transmission line.

19. A circuit for converting a differential current signal to a single-ended signal according to claim 1, further comprising a first direct current source having two terminals and a second direct current source having two terminals,

wherein the bias potential is applied to one of the two terminals of said first direct current source, and the other of the two terminals of said first direct current source is connected to the control terminal of said active device, and

wherein the bias potential is applied to one of the two terminals of said second direct current source, and the other of the two terminals of said second direct current source is connected to the charge-collecting terminal of said active device.

20. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein said active device is a field-effect transistor.

21. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein said active device is a bipolar junction transistor.

22. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein said active device is selected from the group consisting of a metal-semiconductor field-effect transistor, a heterojunction bipolar junction transistor, and a high-electron-mobility transistor.

23. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein at least one among said first and second direct current sources comprises a high-impedance circuit.

24. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein at least one among said first and second direct current sources comprises a resonant circuit having an inductor and a capacitor connected in parallel to said inductor, wherein said resonant circuit has a high impedance.

25. A circuit for converting a differential current signal to a single-ended signal according to claim 19, wherein at least one among said first and second direct current sources comprises a quarter-wavelength transmission line.

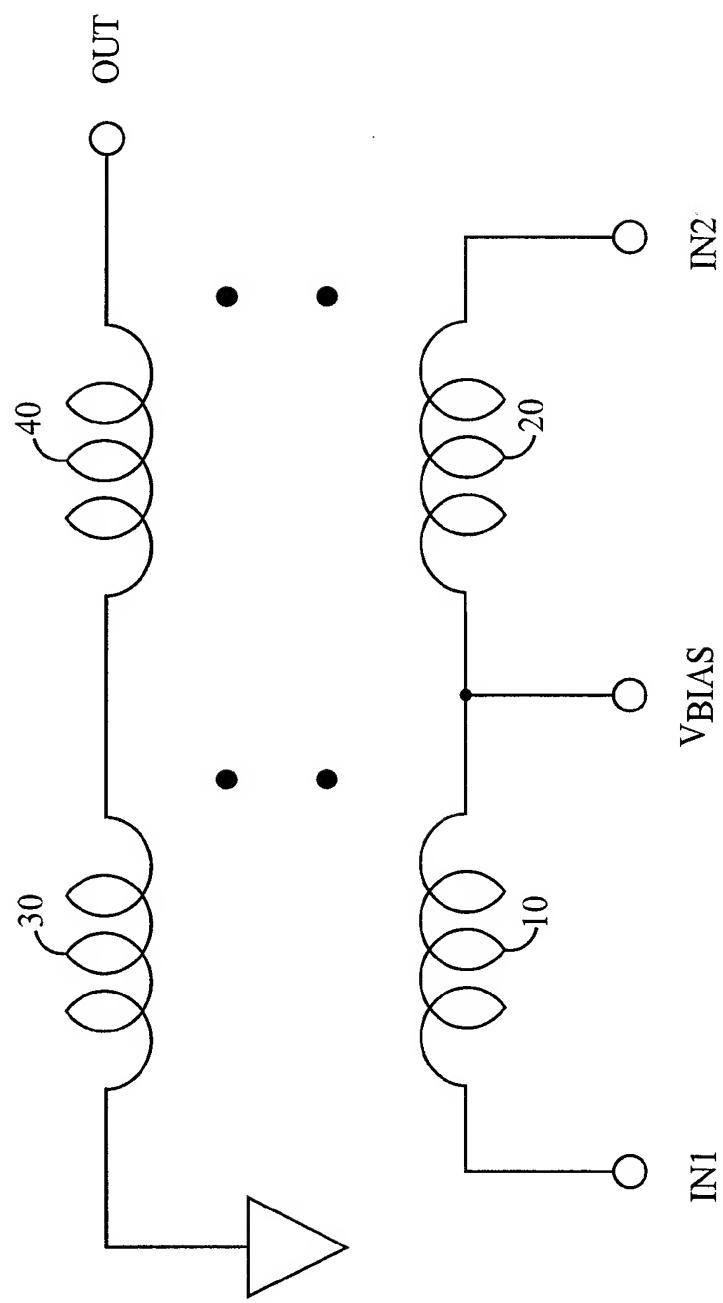


FIG. 1

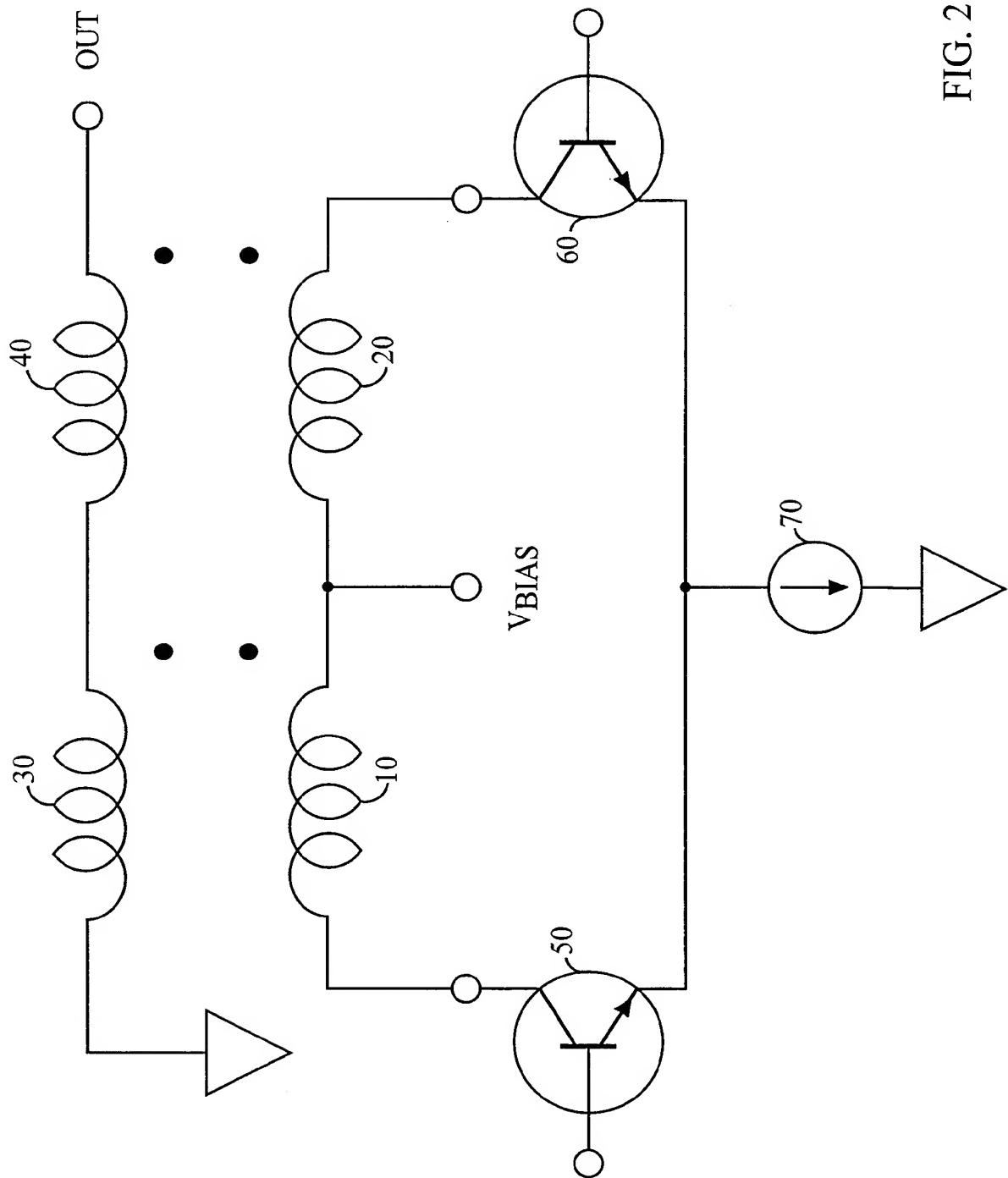


FIG. 2

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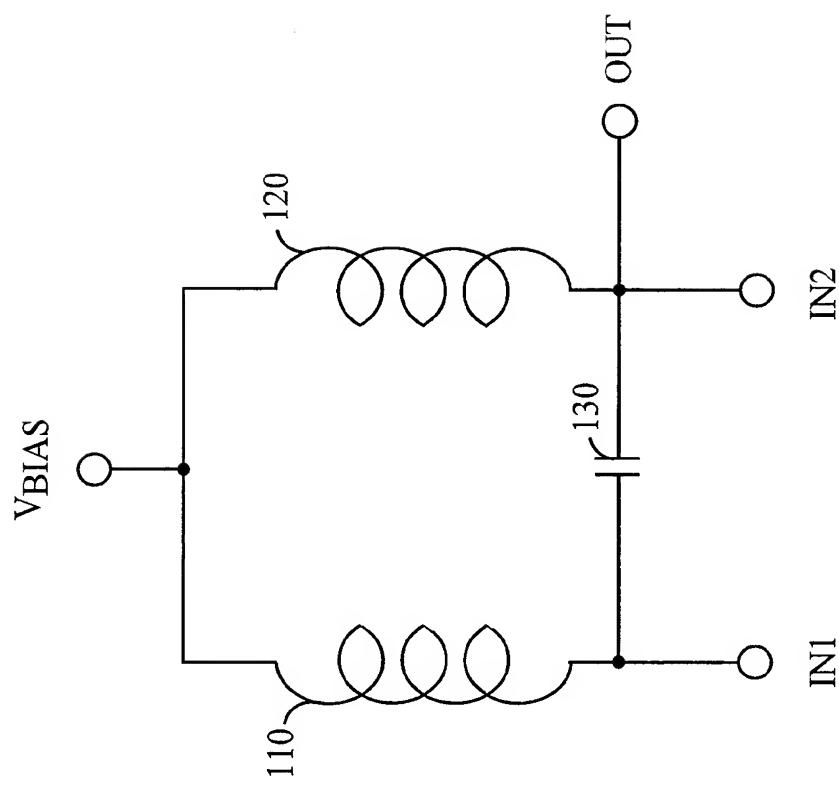


FIG. 3

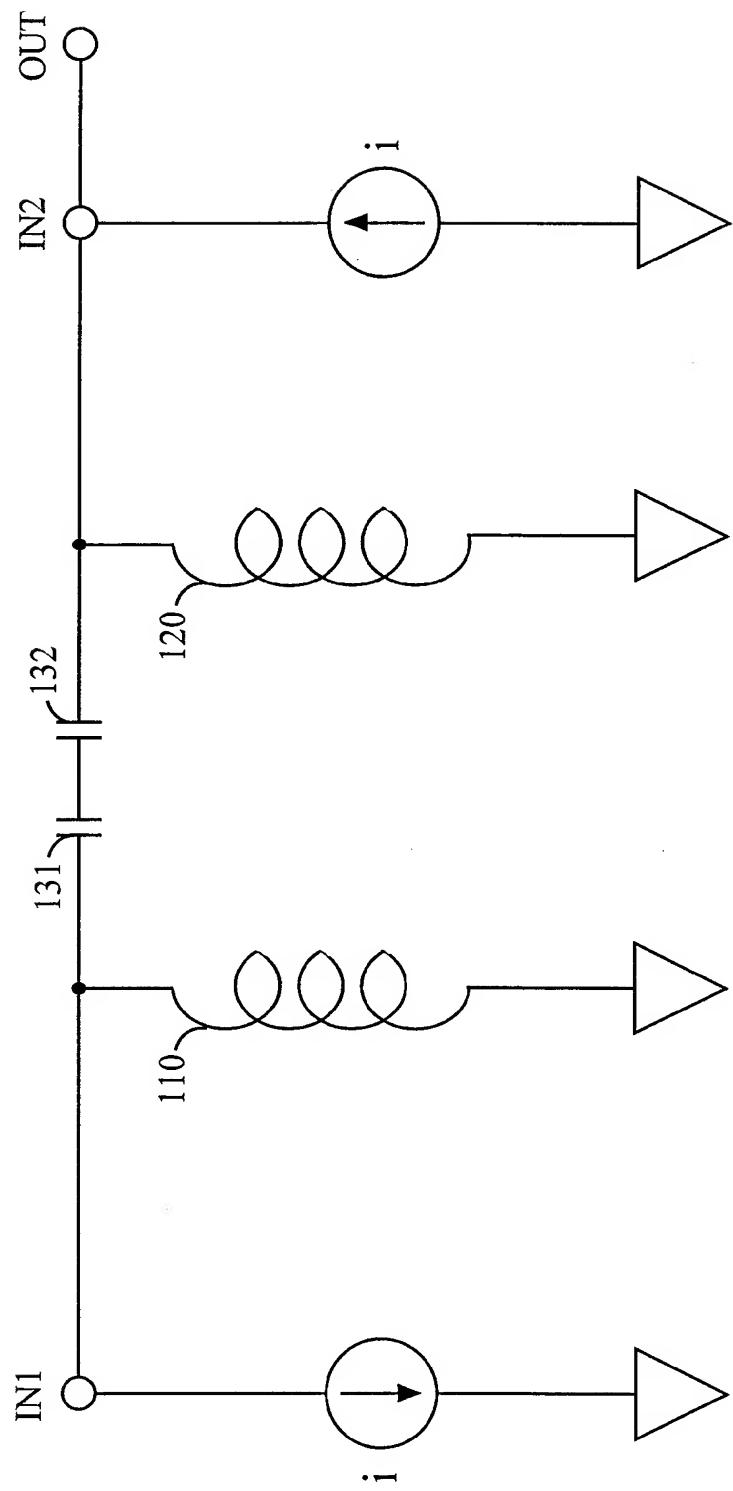


FIG. 4A

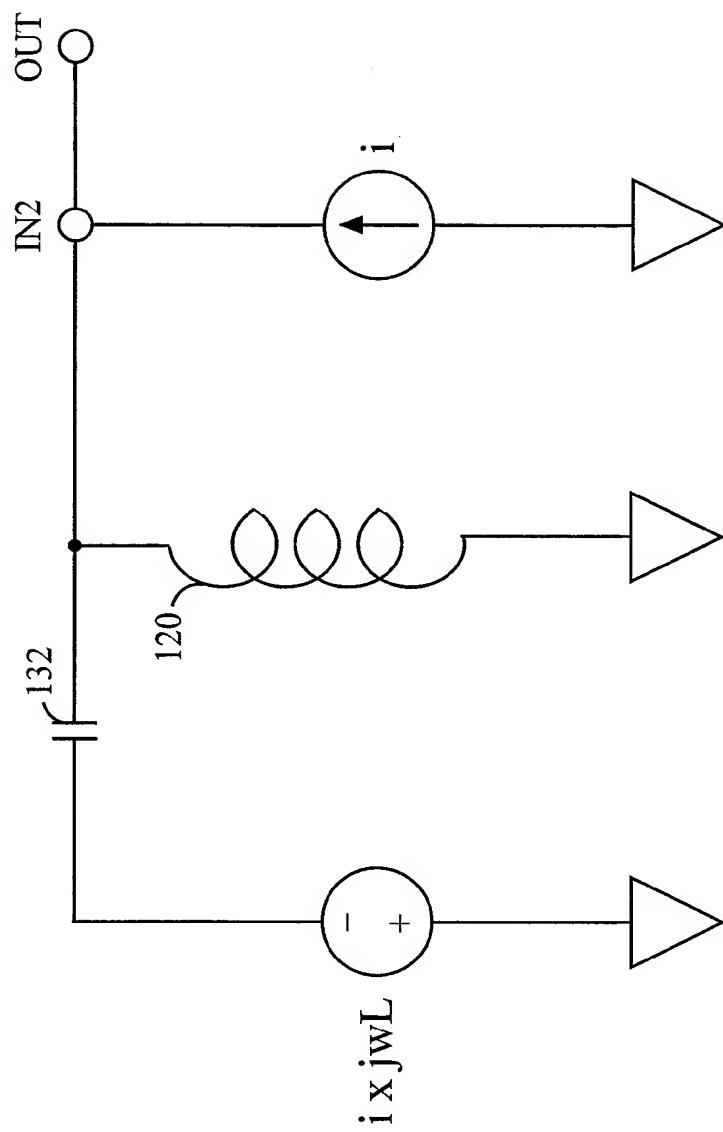


FIG. 4B

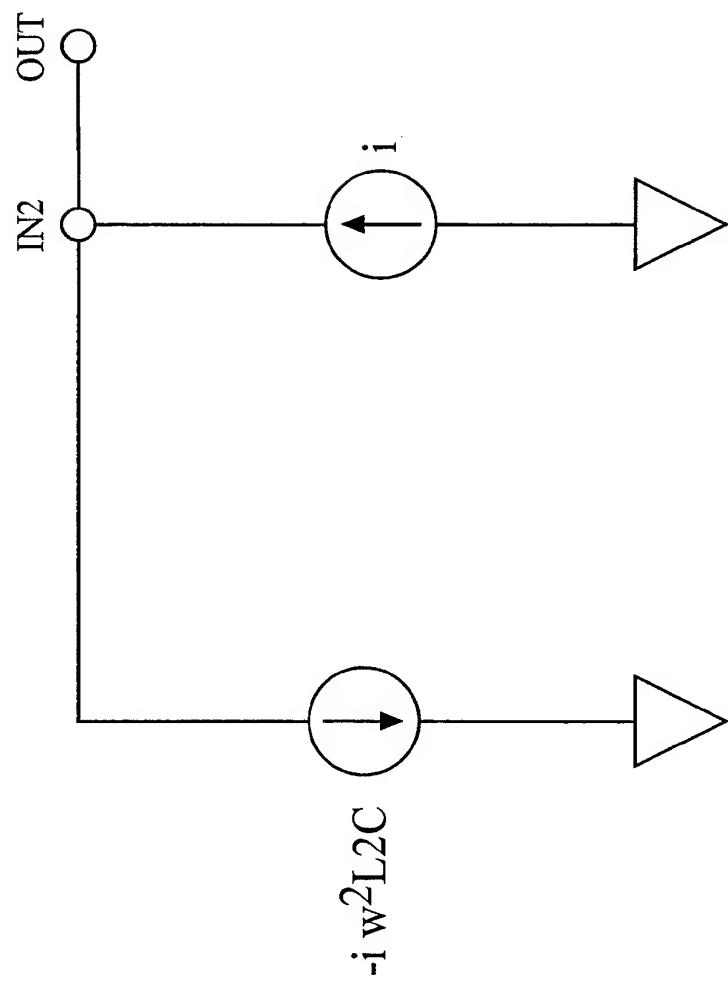


FIG. 4C

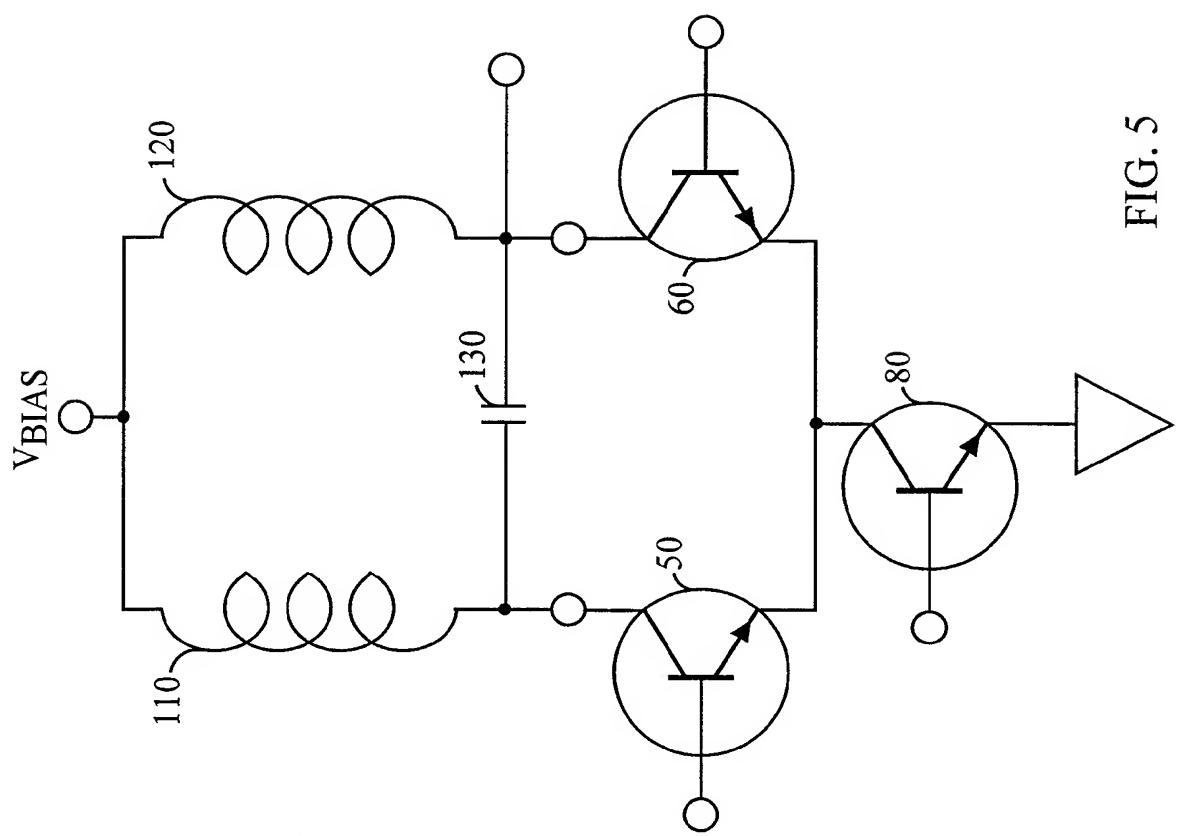


FIG. 5

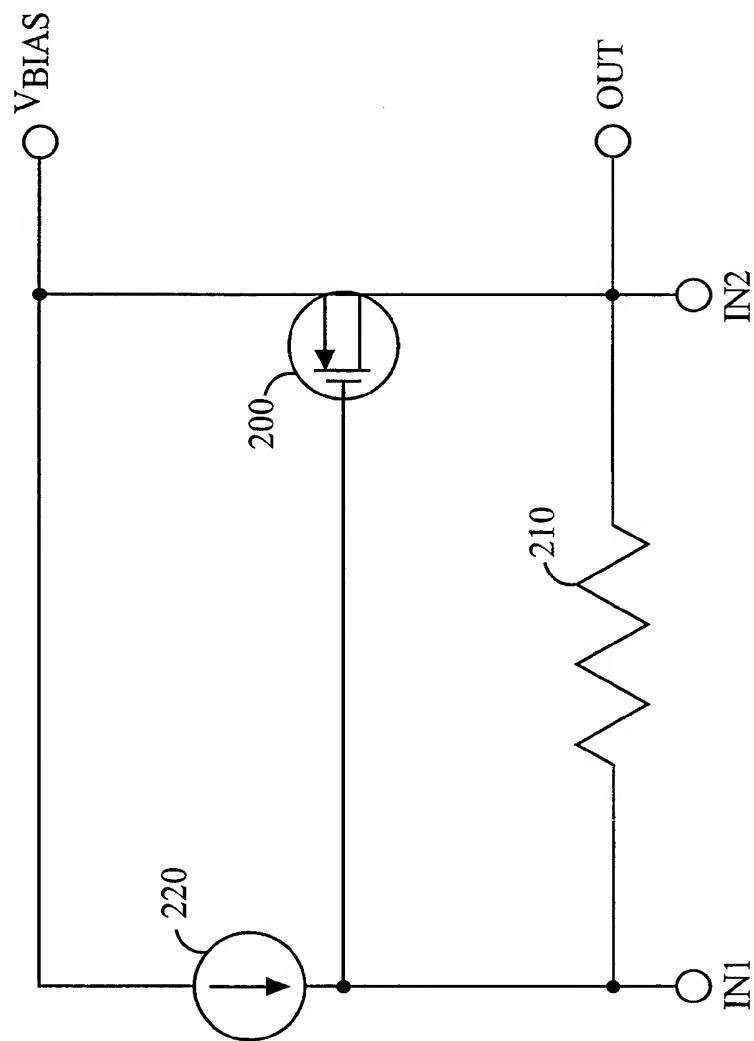


FIG. 6

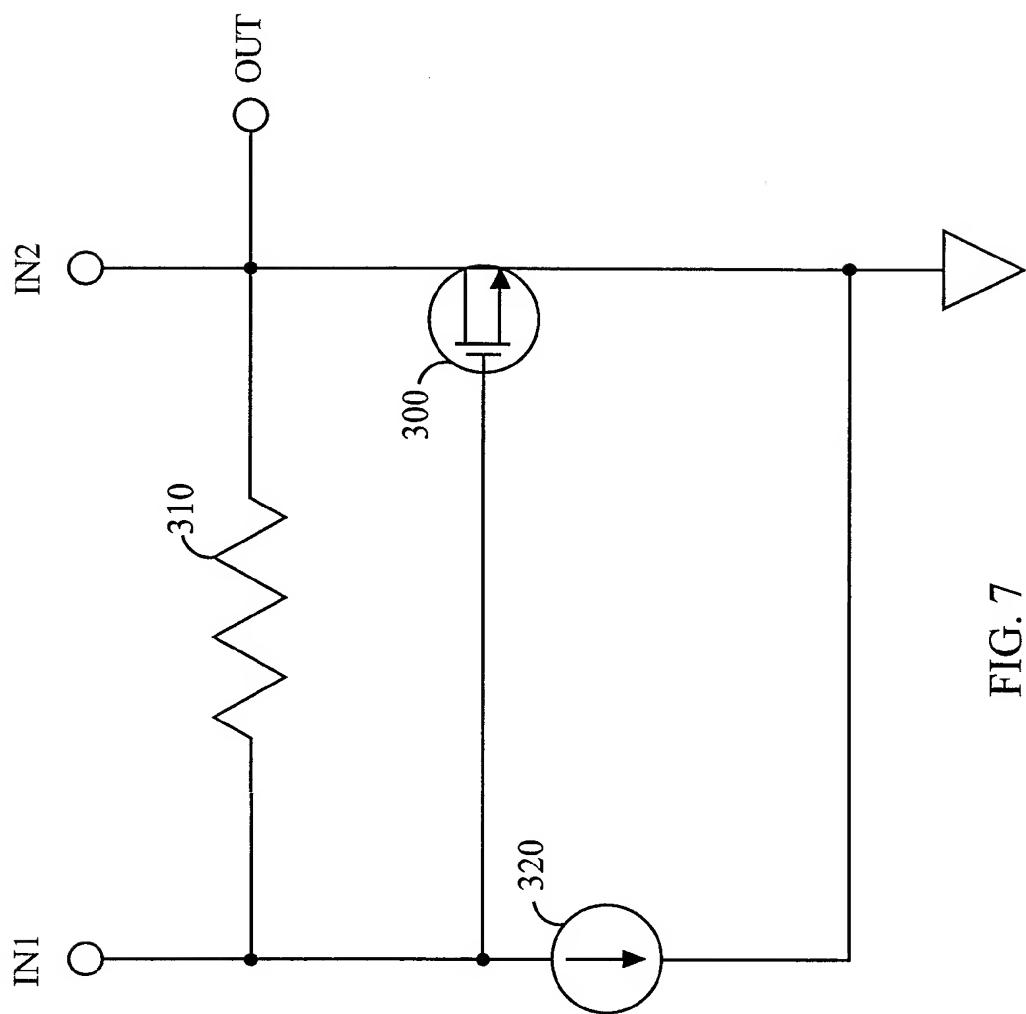


FIG. 7

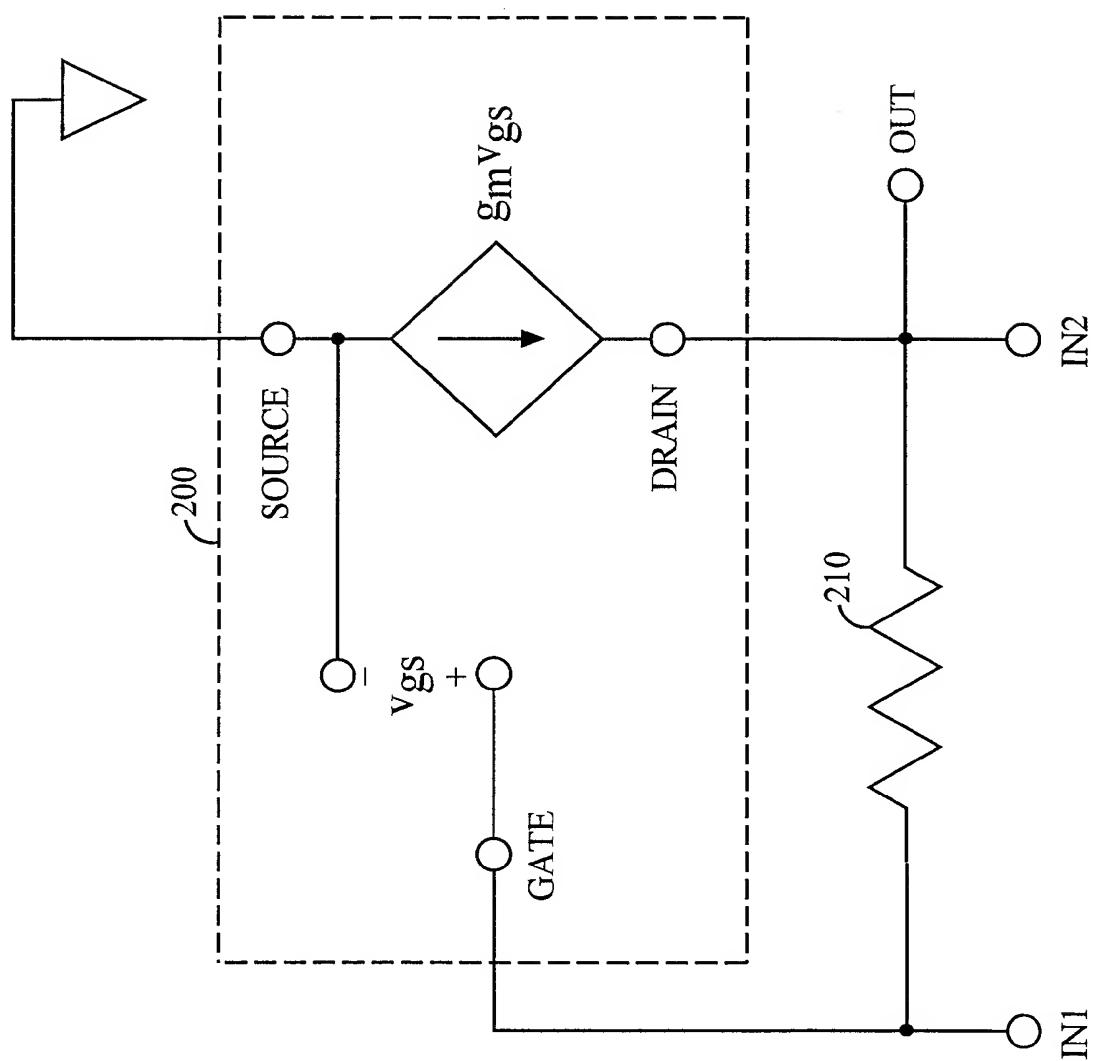


FIG. 8

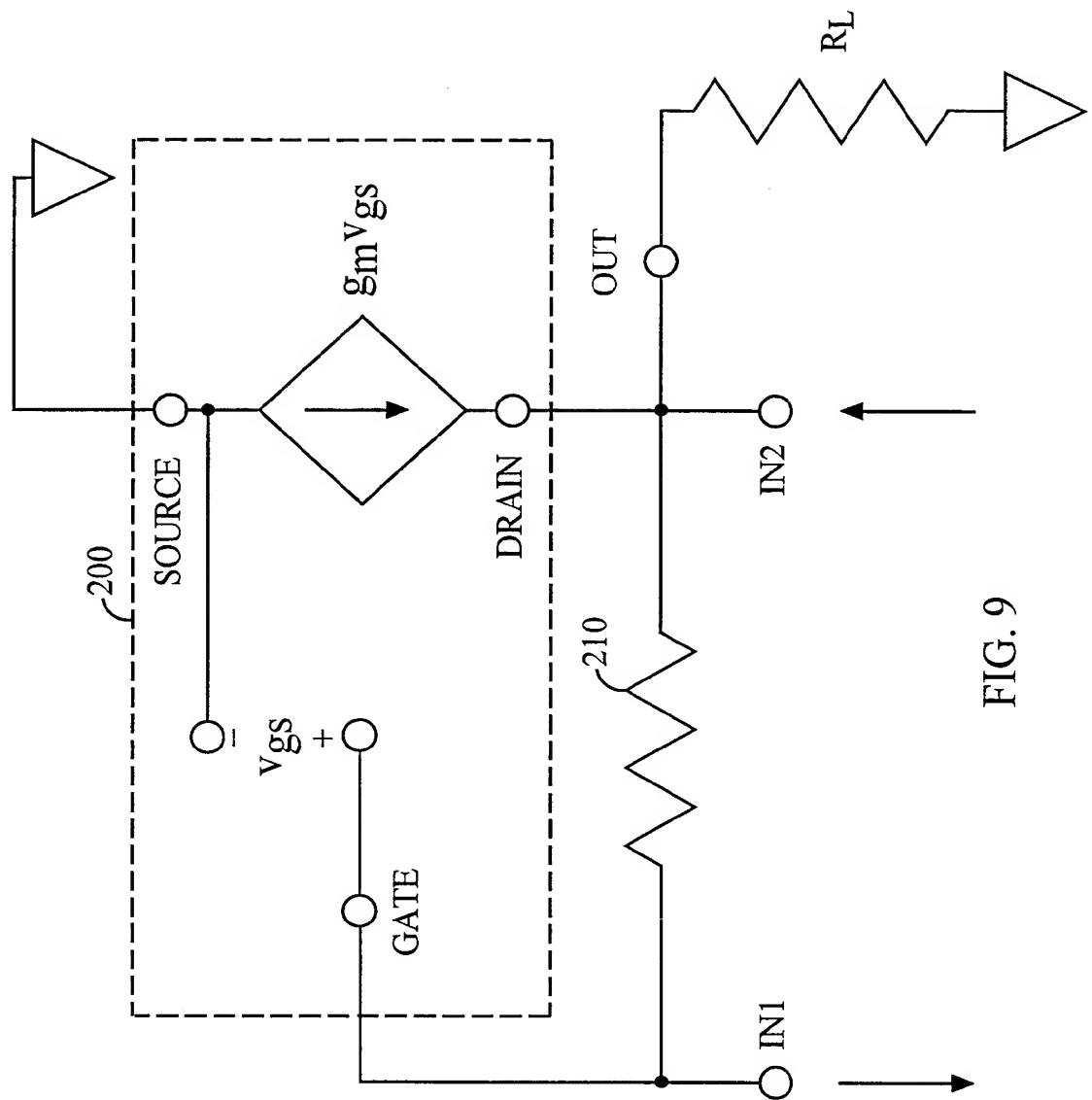


FIG. 9

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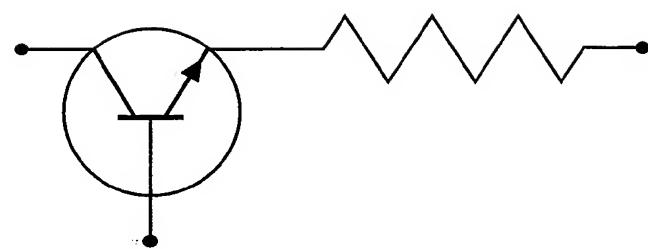


FIG. 11

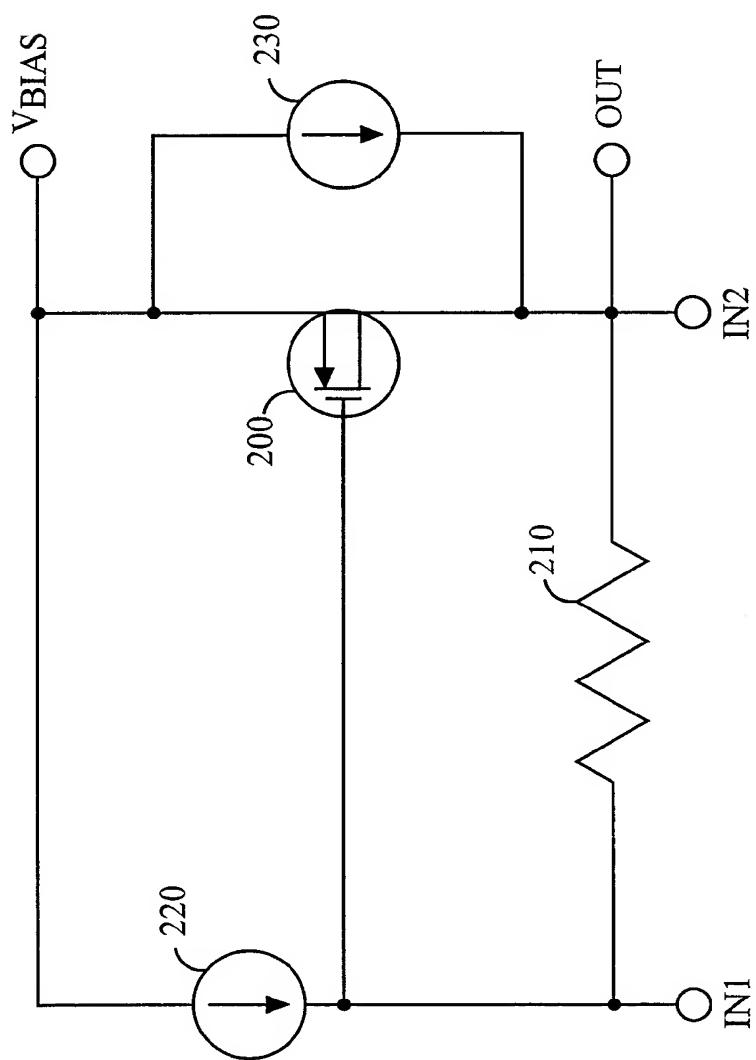


FIG. 10

INTERNATIONAL SEARCH REPORT

International Application No

PCT/US 00/00916

A. CLASSIFICATION OF SUBJECT MATTER

IPC 7 H03F3/45

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC 7 H03F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>PATENT ABSTRACTS OF JAPAN vol. 1995, no. 05, 30 June 1995 (1995-06-30) & JP 07 046061 A (NEC CORP; OTHERS: 01), 14 February 1995 (1995-02-14) abstract</p> <p>-----</p> <p style="text-align: center;">-/--</p>	1



Further documents are listed in the continuation of box C.



Patent family members are listed in annex.

* Special categories of cited documents :

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Date of the actual completion of the international search

16 May 2000

Date of mailing of the International search report

07/06/2000

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	<p>DATABASE INSPEC 'Online! INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB MOKHTARI M ET AL: "Low voltage, broad-and narrowband microwave differential amplifiers for 40 Gb/s-demonstrator applications in InP-HBT" Database accession no. 5723833 XP002137803 abstract; figure 2 & PROCEEDINGS OF 1997 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. CIRCUITS AND SYSTEMS IN THE INFORMATION AGE. ISCAS '97 (CAT. NO.97CH35987), PROCEEDINGS OF 1997 IEEE INTERNATIONAL SYMPOSIUM ON CIRCUITS AND SYSTEMS. CIRCUITS AND SYSTEMS IN TH, pages 149-152 vol.1, 1997, New York, NY, USA, IEEE, USA ISBN: 0-7803-3583-X</p> <p>-----</p>	1
A	<p>DATABASE INSPEC 'Online! INSTITUTE OF ELECTRICAL ENGINEERS, STEVENAGE, GB AKBARI-DILMAGHANI R ET AL: "An RF CMOS differential bandpass amplifier using an active inductor" Database accession no. 6112434 XP002137804 page 1; figures 1,2 & IEE COLLOQUIUM ON SYSTEMS ON A CHIP (REF. NO.1998/439), IEE COLLOQUIUM ON SYSTEMS ON A CHIP, DUBLIN, UK, 5 SEPT. 1998, pages 16/1-6, 1998, London, UK, IEE, UK</p> <p>-----</p>	1

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

PCT/US 00/00916

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
JP 07046061 A	14-02-1995	NONE	